IN THE SPECIFICATION:

Please amend the specification as follows:

Paragraph beginning on page 1, at prenumbered line 15, has been amended as follows:

Thus, the package structure corresponding to the electronic product having high operating frequency is required to have better electrical characteristics so as to stabilize the high-frequency electronic product while functioning. Please refer to Fig. 1, which is a cross-sectional view depicting a package structure of a RF circuit. In the package structure 100 as seen in Fig. 1, the signal transmitted between the chip 110 and the substrate 127 is accomplished using the longer metal wire 125 to couple the chip ~~125~~ 110 with a lead located on the substrate 127. On the other hand, part of the grounding of the signal between the chip 110 and the substrate 127 is accomplished using the shorter metal wire 120 to couple the chip 110 directly with the chip-carrying die pad 130 located on the substrate 127 so that a shorter signal loop between the chip 110 and the substrate 127 can be achieved for enabling the package structure 100 to have better electrical characteristics and heat-flux capability.

Paragraph beginning on page 6, at prenumbered line 5, has been amended as follows:

Please refer to Fig. 3, which is a cross-sectional view depicting a bonding pad structure of a preferred embodiment in accordance to the present invention. As shown in Fig. 3, the bonding pads 210-230 are neighbored with one another and are buried inside the chip 110 from the surface 310 thereof into a depth of its interior. From the surface 310 of the chip 110 to the interior thereof, the bonding pads 210-230 respectively comprise a plurality of metal plates 320-360 and a plurality of plugs 365-373 that are successively superimposed to one another, moreover, the amount and the order of the plates and the plugs are depended on the amount of metal layers installed in the chip 110 (i.e. 6 layers in the chip 110).

Paragraph beginning on page 6, at prenumbered line 15, has been amended as follows:

That is, the bonding pad 210 is formed, successively from the surface 310 of the chip 110 to the interior thereof, with a plug 365, a metal plate 320, a plug 366, a metal plate 330, a plug 367 and a metal plate 340. Similarly, the bonding pad 220 is formed with a metal plate ~~345~~ 220, a plug 368, a metal plate ~~349~~ 347, a plug 369, a metal plate 348 and a plug 370. Similarly, the bonding pad 230 is formed with a plug 371, a metal plate 349, a plug 372, a metal plate 350, a plug 373 and a metal plate 360.

Paragraph beginning on page 6, at prenumbered line 31, has been amended as follows:

Wherein, the characteristic of the bonding pad structure 210-230 is that the metal plates 320-340 of the bonding pad 210 and the metal plates ~~345-345~~ 347-348 of the bonding pad 220 are parallel extending toward each other, and a portion thereof are overlapping with one another, also every two intersecting metal plates is positioned apart from each other with a distance d so that a parallel metal plate structure 380 is formed. Thus, as seen in Fig. 3, the parallel metal plate structure 380 between the bonding pads 210 and 220 is constructed successively using the metal plate 320, the metal plate 347, the metal plate 330, the metal plate 348 and the metal plate 340, also the metal structure 380 contains insulation layers 112 in-between metal plates, such as SiO_2.

Paragraph beginning on page 7, at prenumbered line 8, has been amended as follows:

Similarly, the metal plates ~~345-348~~ 347-348 of the bonding pad 220 and the metal plates 349-360 of the bonding pad 230 are parallel extending toward each other, and a portion thereof are overlapping with one another, also every two intersecting metal plates is positioned apart from each other with a distance d so that a parallel metal plate structure 390 is formed. Thus, as seen in Fig. 3, the parallel metal plate structure 390 between the bonding pads 220 and 230 is constructed

successively using the metal plate 349, the metal plate 347, the metal plate 350, the metal plate 348 and the metal plate 360.

Paragraph beginning on page 7, at prenumbered line 17, has been amended as follows:

Since the bonding pad structure comprising the bonding pads 210-230 has the two parallel metal plate structures 380 and 390 existing in-between bonding pads, when the metal plates ~~350-360~~ 320-360 respectively within the bonding pads 210-230 are used by the chip 110 to transmit signals to the metal layers M1-M6 within the chip 110, one who skilled in the art will know that the two parallel metal plate structures 380 and 390 existing in the bonding pad structure 210-230 will increase the capacitance of the loop inside the chip 110.

Paragraph beginning on page 8, at prenumbered line 1, has been amended as follows:

From experiment, when the chip 110 of Fig. 1 uses the bonding pads 210-230 ~~pf~~ of the present invention, the electrical performance is optimized, that is, the ~~return~~ insertion loss and the ~~insertion~~ return loss will approach an optimum value. Please refer to Fig. 5, Fig. 6A and Fig. 6B, which respectively are a reference table, and reference charts showing the ~~return~~ insertion loss (S11) and the return ~~insertion~~ loss (S12) of the package structure of Fig. 1 before and after using the bonding pad structure 210-230 of the present invention.

Paragraph beginning on page 8, at prenumbered line 20, has been amended as follows:

Therefore, the ~~return~~ insertion loss of the total loop of the package structure 100 is ~~increased~~ decreased after using the bonding pad structure 210-230 of the present invention, and the ~~insertion~~ return loss of the total loop of the package structure 100 is ~~decreased~~ increased after using the bonding pad structure 210-230 of the present invention. The decrease of the insertion loss is helpful to the package structure 100 for reducing energy loss and enhancing signal integrity of high-frequency signal. Thus, the distribution of the return loss and the insertion loss of the

total loop can be optimized using the bonding pad structure 210-230 of the present invention.